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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,999	12/22/2000	Richard P. Modelski	P 269864 NOR- 13164BA	7780

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EXAMINER	
MAHMOUDI, HASSAN	
ART UNIT	**PAPER NUMBER**
2175	14

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/741,999	Applicant(s) MODELSKI ET AL.	
	Examiner Tony Mahmoudi	Art Unit 2175	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

DOV POPOVICI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. In response to communications filed on 29-April-2004, claim 17 is cancelled, and the specification of the disclosure and claims 1, 5, and 9 are amended per applicant's request. Therefore, claims 1-16 and 18 are presently pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-6, 9-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narad et al (U.S. Patent No. 6,157,955) in view of Christie et al (U.S. Patent No. 6,157,996.)

As to claim 1, Narad et al teaches a method for direct access to bit fields in instruction operands (see Abstract, and see column 11, lines 12-24), the method comprising:

providing bit fields (see column 22, lines 9-15) in a processor executable instruction (see column 3, lines 66-67, and see column 10, lines 32-33), each of the bit fields consisting of a plurality of bits in a plurality of bit positions (see column 22, lines 9-45, and see TABLE 1);

performing the processor executable instruction utilizing the bit fields in the source and target operands in response to the bit fields (see column 27, lines 4-7, and see column 28, lines 17-24); and

providing, by the performing the processor executable instruction, and in response to the bit fields, direct manipulation of any bits in any bit field (see column 24, lines 50-64, and see column 59, lines 39-50.)

Narad et al does not teach:

indications of bit fields in source and target operands; and

manipulation of bits in any bit field of the source and target operands.

Christie et al teaches a processor for executing computer instructions (see Abstract), in which he teaches:

indications of bit fields in source and target operands (see column 3, lines 23-31, see column 5, lines 19-32, see column 7, lines 8-29, and see column 17, lines 4-13) ; and

manipulation of bits in any bit field of the source and target operands (see column 3, lines 9-12, and see column 7, lines 13-29.)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Narad et al to include indications of bit fields in source and target operands; and manipulation of bits in any bit field of the source and target operands.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Narad et al by the teachings of Christie et al, because including indications of bit fields in source and target operands; and manipulation of bits in

any bit field of the source and target operands, would provide the advantage of indicating bit fields and manipulating bit fields in any of the source or destination operands, and storing the results of the bit-manipulations in a third operand, as taught by Christie et al (see column 3, lines 9-12.)

As to claim 2, Narad et al as modified, teaches the method further comprising:

transferring data from an input buffer to a packet task manager (see Narad et al, column 9, lines 11-26, and see column 15, lines 14-18);

dispatching the data from the packet task manager to an analysis machine (see Narad et al, column 13, lines 14-43, and see column 36, lines 40-45);

classifying the data in the analysis machine (see Narad et al, column 37, lines 15-26); and

modifying (see Narad et al, column 31, lines 29-32) and forwarding the data in a packet manipulator (see Narad et al, column 31, lines 35-53);

wherein no instruction depends on a preceding instruction because each instruction in a pipeline is executed for a different thread (see Narad et al, column 37, line 63 through column 38, line 3, and see column 41, lines 50-55.)

As to claim 3, Narad et al as modified, teaches the method further comprising:

transferring the data after modifying and forwarding to an output buffer (see Narad et al, column 9, lines 1-27.)

As to claim 5, Narad et al teaches an apparatus for directly accessing bit fields in instruction operands (see Abstract, and see column 11, lines 12-24), the apparatus comprising:

at least one memory (see figure 4, see column 7, lines 14-15, and see column 8, lines 12-15);

at least one processor (see column 8, lines 38-39);

a bus interconnecting the at least one memory and the at least one processor (see figure 3, and see column 7, lines 26-31);

wherein one of the at least one processor retrieves bit fields consisting of a plurality of bits in a plurality of bit positions (see column 22, lines 9-45, and see column 43, lines 56-60) for a processor executable instruction (see column 3, lines 66-67, and see column 10, lines 32-33), performs the processor executable instruction utilizing the bit fields in source and target operands in response to the bit fields (see column 27, lines 4-7, and see column 28, lines 17-24), and provides, by performance of processor executable instruction, and in response to the bit fields, direct manipulation of any bits in any bit field (see column 24, lines 50-64, and see column 59, lines 39-50.)

for the teaching of "indications of bit fields in source and target operands; and manipulation of bits in any bit field of the source and target operands", the applicant is kindly directed to the remarks and discussions made in claim 1 above.

As to claim 6, Narad et al as modified, teaches wherein the processor comprises:

an analysis machine having multiple pipelines (see Narad et al, column 3, lines 56-65);

a packet task manager operationally connected to the analysis machine (see Narad et al, column 14, lines 53-63); and,

a packet manipulator operationally connected to the analysis machine (see Narad et al, column 59, line 39 through column 60, line 10.)

As to claim 9, Narad et al as modified, teaches the apparatus further comprising:

a packet task manager operationally connected to the analysis machine (see Narad et al, column 14, lines 53-63);

a packet manipulator operationally connected to the analysis machine (see Narad et al, column 59, line 39 through column 60, line 10); and

a global access bus including a master request bus and a slave request bus separated from each other and pipelined (see Narad et al, figure 3, and see column 7, lines 26-31.)

As to claim 10, Narad et al as modified, teaches the apparatus further comprising:

an external memory engine operationally connected to the analysis machine (see Narad et al, column 7, lines 63-67); and

a hash engine operationally connected to the analysis machine (see Narad et al, column 4, lines 52-53, and see column 6, line 62 through column 7, line 2.)

As to claims 11 and 12, Narad et al as modified, teaches the apparatus further comprising:

packet input global access bus software code used for flow of data packet information from a flexible input data buffer to an analysis machine (see Narad et al, figure 2, see column 32, lines 1-7, and see column 33, lines 64-67.)

As to claim 13, Narad et al as modified, teaches the apparatus further comprising:

statistics data global access bus software code used for connection of an analysis machine to a packet manipulator (see Narad et al, column 8, lines 15-20, and see column 15, lines 21-22.)

As to claim 14, Narad et al as modified, teaches the apparatus further comprising:

private data global access bus software code used for connection of an analysis machine to an internal memory engine submodule (see Narad et al, column 12, line 50 through column 13, line 13.)

As to claim 15, Narad et al as modified, teaches the apparatus further comprising:

lookup global access bus software code used for connection of an analysis machine to an internal memory engine submodule (see Narad et al, column 36, lines 40-45.)

As to claim 16, Narad et al as modified, teaches the apparatus further comprising:

results global access bus software code used for providing flexible access to an external memory (see Narad et al, column 36, lines 46-58.)

As to claim 18, Narad et al as modified, teaches the apparatus further comprising:

a bi-directional access port operationally connected to the analysis machine (see Narad et al, column 104, lines 50-62);

a flexible data input buffer operationally connected to the analysis machine (see Narad et al, column 15, lines 14-18); and

a flexible data output buffer operationally connected to the analysis machine (see Narad et al, column 16, lines 26-30.)

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Narad et al (U.S. Patent No. 6,157,955) in view of Christie et al (U.S. Patent No. 6,157,996), as applied to claims 1-3, 5-6, 9-16, and 18 above, and further in view of Islam et al (U.S. Publication No. 2003/0035430 A1.)

As to claim 4, Narad et al as modified, teaches the method further comprising:

processing data (see Narad et al, Abstract.)

Narad et al as modified, still does not teach processing data at a rate of at least 10 Gbs.

Islam et al teaches a programmable network device (see Abstract), in which he teaches processing data at a rate of at least 10 Gbs (see paragraph 43.)

Therefore, it would have been obvious to a person having ordinary skill in the art to have modified Narad et al as modified, to include processing data at a rate of at least 10 Gbs.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Narad et al as modified, by the teaching of Islam et al,

because processing data at a rate of at least 10 Gbs, would enhance the processing speed of the data and reduce the processing time and the load on the data networks.

5. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narad et al (U.S. Patent No. 6,157,955) in view of Christie et al (U.S. Patent No. 6,157,996), as applied to claims 1-3, 5-6, 9-16, and 18 above, and further in view of Stuttard et al (U.S. Publication No. 2002/0174318 A1.)

As to claim 7, Narad et al as modified, still does not teach wherein the analysis machine is multi-threaded.

Stuttard et al teaches a parallel data processing apparatus (see Abstract), in which he teaches wherein the analysis machine is multi-threaded (see paragraphs 49-50.)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Narad et al as modified, to include wherein the analysis machine is multi-threaded.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Narad et al as modified, by the teaching of Stuttard et al, because wherein the analysis machine is multi-threaded, would enable concurrent processing of multiple tasks simultaneously.

As to claim 8, Narad et al as modified, teaches wherein the analysis machine has 32 threads (see Stuttard et al, paragraph 153.)

Response to Arguments

6. Applicant's arguments filed on 29-April-2004 with respect to the rejected claims in view of the cited references have been fully considered but they are moot in view of the new grounds for rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiries concerning this communication or earlier communications from the examiner should be directed to Tony Mahmoudi whose telephone number is (703) 305-4887. The examiner can normally be reached on Mondays-Fridays from 08:00 am to 04:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici, can be reached at (703) 305-3830.

tm

June 25, 2004

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